

**Understanding and Improving the Metal-Semiconductor Interface
of 2D MoS₂-based Schottky Junctions**

A THESIS SUBMITTED ON THE THIRTEENTH DAY OF MAY 2021
TO THE DEPARTMENT OF PHYSICS AND ENGINEERING PHYSICS
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
OF THE SCHOOL AND SCIENCE AND ENGINEERING

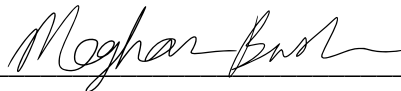
OF TULANE UNIVERSITY

FOR THE DEGREE

OF

MASTER OF SCIENCE

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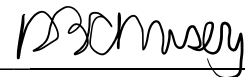


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ACKNOWLEDGEMENTS

Thank you to the funders of this project:

- The Newcomb Institute at Tulane University, as part of a Faculty Research grant
- The Louisiana BOR, as part of a NASA EPScoR grant
- The NSF, who funded the electron-beam lithography tool

I would also like to give a big thank you to my lab mates Kazi, Tim, and Claire for being an awesome team to work with.

1. INTRODUCTION

1.1. 2D Materials

The discovery of graphene by graphite exfoliation in 2004 led to the emergence of a new field in materials science: fabrication two-dimensional (2D) materials that consist of a single atomic layer. While atoms within the same plane are subjected to strong covalent bonding, weak Van der Waals bonding between layers allows these materials to be easily separated by atomic layer.

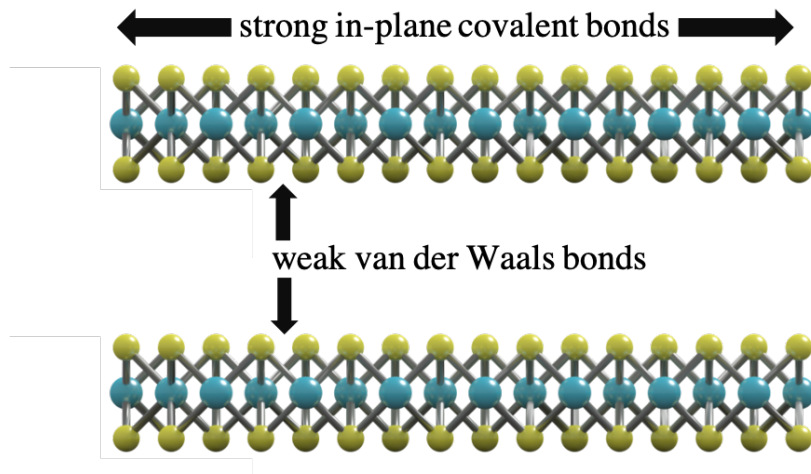


Figure 1: van der Waals bonding in 2D materials

These monolayer materials were shown to have new exciting properties differing from their bulk material counterparts. One subgroup are the transition metal dichalcogenides (TMDCs), which are made up of transition metal atom (M) and chalcogen atom (X) in the form MX_2 . In particular, molybdenum disulfide (MoS_2) exhibits a shift from an indirect bandgap in bulk to a direct bandgap in monolayer^{2, 3}. The bandgap of a semiconductor

indicates whether electron excitation to a higher state involves a change in particle momentum, or the k-space.

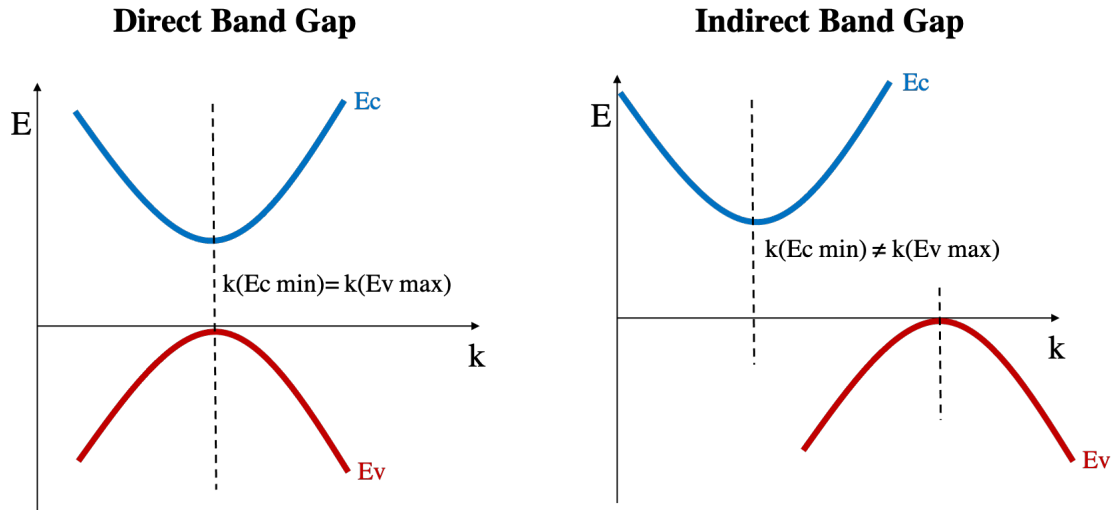


Figure 2: E-k diagram comparing a direct and indirect bandgap

Direct bandgap materials are well-suited for optical uses due to the ease of carrier excitation. Electrons can be directly excited into the conduction band of a crystal without additional energy or phonon emission, which will introduce unwanted heat.

While exfoliation was initially the only means of producing 2D materials, researchers are now finding ways to ways to grow these films. One such method is chemical vapor deposition, or CVD; this method works by heating a precursor so that it evaporates and travels along an isolated tube via an inert carrier gas. The gaseous solution interacts with a substrate and nucleation occurs on both faces.

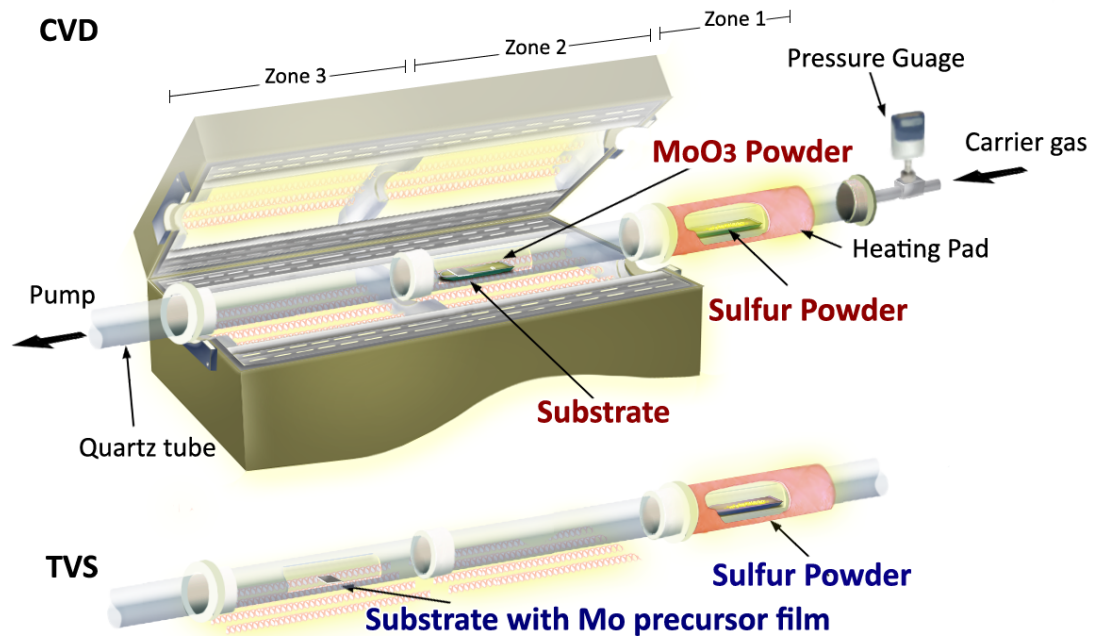


Figure 3: Chemical vapor deposition setup²⁰

The specific process used in the Escarra group is as follows:

- a) SiO₂ substrate mounted in crucible in Zone 2.
- b) The system is pumped down to 2.4 torr.
- c) Sulfur powder is heated to 140°C in Zone 1 over 30 minutes. Once evaporated, it is picked up by the argon carrier gas, which flows at roughly 160 sccm.
- d) Zone 2 is also heated to 750C over 30 minutes. Sulfur-argon flows into Zone 2, where it interacts with the MoO₃.
- e) Temperature is maintained for 10 minutes while MoO₃ and S nucleate on substrate to form MoS₂ film. Initial flakes coalesce into a monolayer film.
- f) System is allowed to cool to room temperature and substrate is removed.

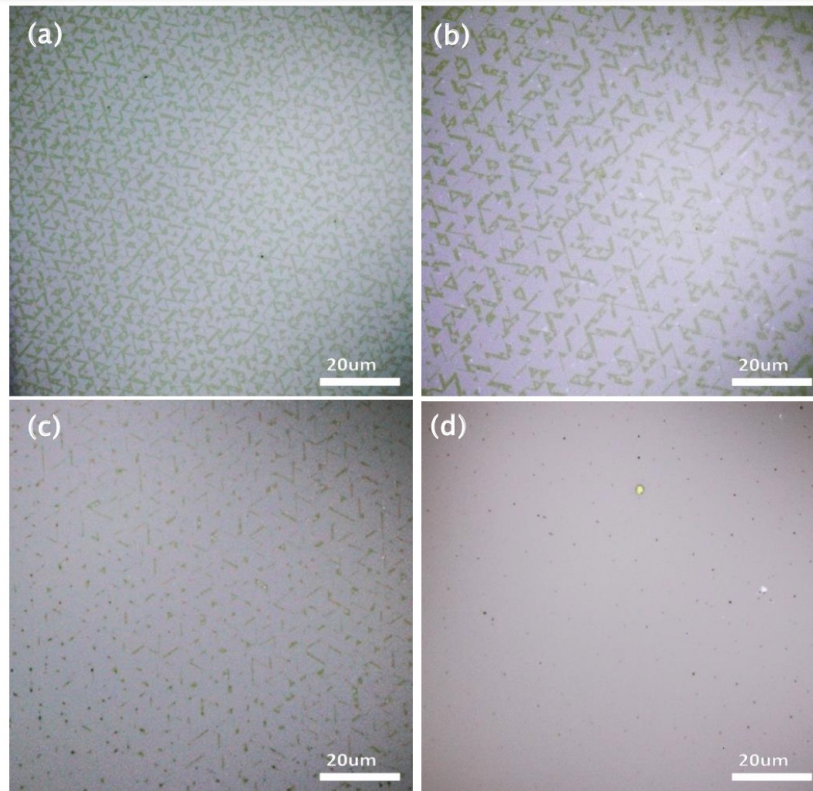


Figure 4: MoS₂ flakes coalescing into monolayer film during CVD growth

These films are characterized using photoluminescence mapping (to quantify photocurrent generation and electrical sensitivity) Raman spectroscopy (to confirm the number of layers present).

1.2. Photovoltaic Devices

Photovoltaic (PV) devices, commonly known as solar cells, convert incoming light energy into electricity using the photoelectric effect. A typical device will have a base and emitter layer; emitters are typically much smaller than the base. For this explanation, assume the emitter is n-type and the base is p-type. Metal contacts sandwich the

semiconductors. Photons are incident on the emitter and generate an electron-hole pair of the same energy. The electron travels through n-type emitter, is collected by the contact, and travels through the circuit to the metal contact on the base. The hole travels through the p-type base, where it recombines with the electron. This carrier movement generates a current called photocurrent, since it is created by incident photons.^{12, 19}

1.3. 2D PV Devices

While traditional solar cells like Si and III-V are still being improved on by research groups, the Escarra group is exploring the world of solar cells fabricated using 2D films, or 2D PV. These devices present very compelling advantages to traditional solar. For one, they have a specific power orders of magnitude higher than GaAs and Si.

Material	Thickness	Efficiency (%)	Weight	Power Density (g/m ²)
GaAs	1 μm	~29	5.3	290
Si	25 μm	20.6	92.7	5.9
Graphene/MoS₂	0.9 nm	0.1 – 1.0	3.9e-3	1000 – 10000
WS₂/MoS₂	1.2 nm	0.4 – 1.5	7.9e-3	3000 - 12000

Table 1: Material property comparison of common solar cells¹

MoS₂'s bandgap goes from indirect to direct when going from bulk to monolayer, indicating potential for photonic applications. It has an ultrathin form factor and requires significantly less mass for operation. This makes it attractive for markets that are constrained by mass or weight, such as aerospace.

Using chemical vapor deposition instead of exfoliation is a scalable manufacturing process and allows for large-area synthesis. Being able to mass produce cells is an important factor to consider since it can prevent high efficiency cells from hitting the market due to economic concerns.

A crucial part of photovoltaic devices is their ability to separate electrons and holes to be collected at opposite contacts. This can be achieved in 2D PV devices using asymmetric Schottky contacts, as shown in Figure 6.

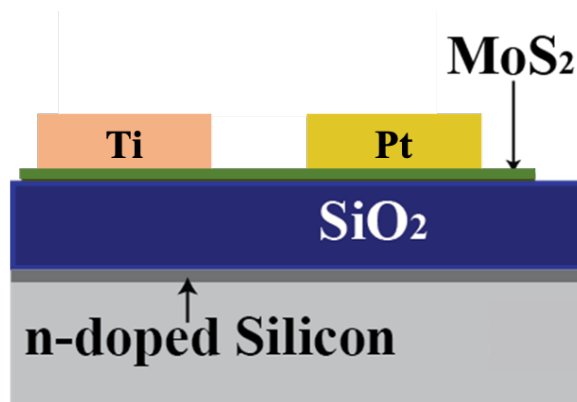


Figure 6: 2D PV device architecture; metal contacts top monolayer MoS₂, a sapphire substrate, and an n-doped silicon base.

The metals used for the asymmetric contacts are chosen based on their work function. A metal with a higher work function will be more likely to gather holes, while a metal with a low work function will be more likely to gather electrons. The contacts are designed with interlocking fingers. Electron-hole pairs are excited by incident light in the exposed MoS₂ then gathered by their respective contact. Transport and solar cell function depend on the interface between the metal and semiconductor.

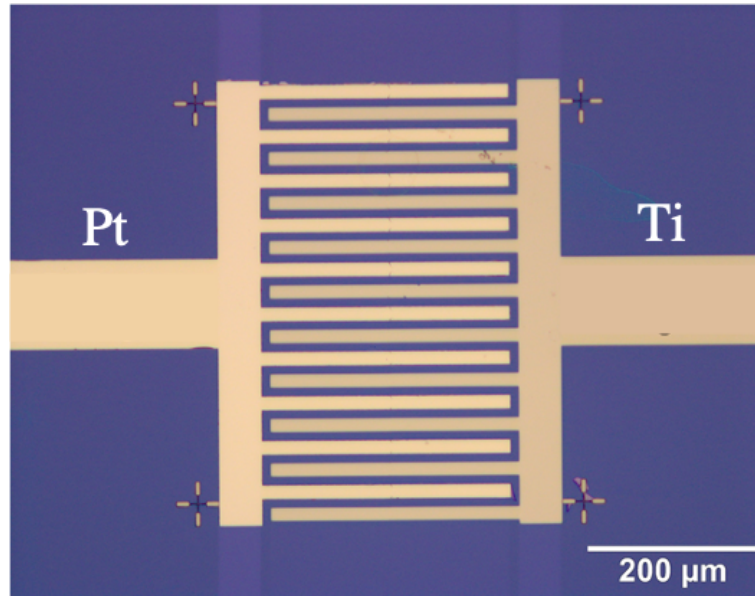


Figure 7: Optical microscope image of a 2D PV device with interlocking platinum and titanium fingers.

1.4. Explanation of Metal-Semiconductor Interface

For a semiconductor to interact with other circuit elements, metal contacts must be fabricated and connected. The metal-semiconductor interface has unique properties based on the characteristics of both materials. For a metal-semiconductor junction, there are two possible contacts: Ohmic or Schottky barrier.

1.2.1 Ohmic Contact

An Ohmic contact is a nonrectifying barrier, meaning it is designed to allow electrons to easily flow from the semiconductor to the metal contact for collection. Carriers move in both directions without impedance and are not slowed by large potential differences. This kind of barrier is ideal for carrier collection without modulation. The band structure of this interface is shown in Figure 8.

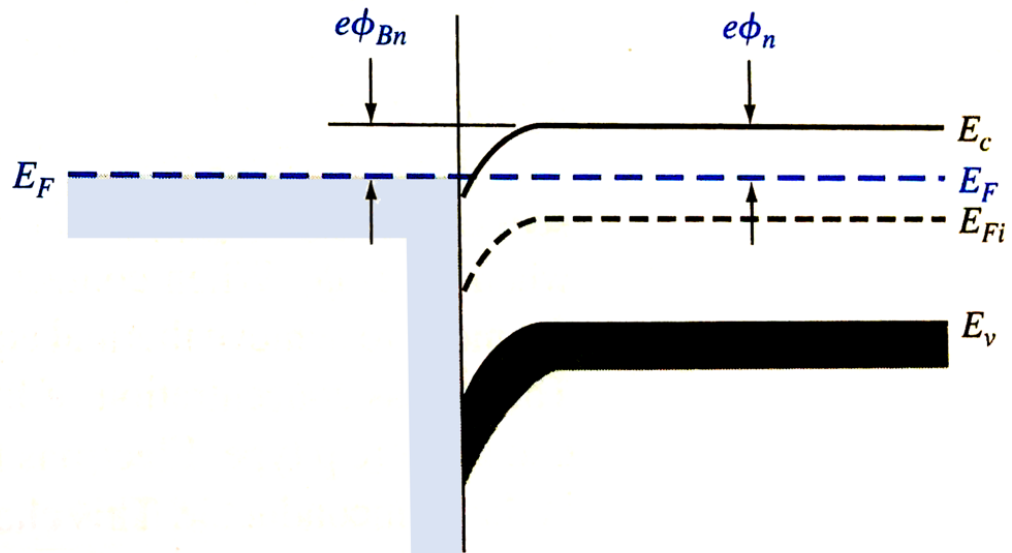


Figure 8: Band structure of an Ohmic contact at a metal-semiconductor interface¹²

Ohmic contacts are in accordance with Ohm's law and display a linear relationship between current and voltage. Because of this, they are very sensitive to resistance. Specific resistance, R_c , is used to compare contact performance. This resistance decreases with a decrease in barrier height according to Equation 1¹².

$$R_c = \frac{\frac{kT}{e} \exp\left(\frac{+e\phi_{Bn}}{kT}\right)}{A^*T^2} \quad (\text{Eqn. 1})$$

Ohmic contacts are ideal for connecting semiconductor devices within a circuit since they do not have a significant impact to transport. However, when selective carrier separation is desired, a different type of metal contact must be used.

1.2.2 Schottky Contact

A Schottky contact is a rectifying barrier that exists between a metal and semiconductor with a significant potential difference at the interface. This potential is known as the Schottky barrier and is a function of the semiconductor's electron affinity (χ_s) and the work function (ϕ_m) of the metal¹², as seen in Equation 2.

$$\phi_{B0} = (\phi_m - \chi_s) \quad (\text{Eqn. 2})$$

In thermal equilibrium, the Fermi level of the metal and semiconductor are equivalent, resulting in the band structure in Figure 9.

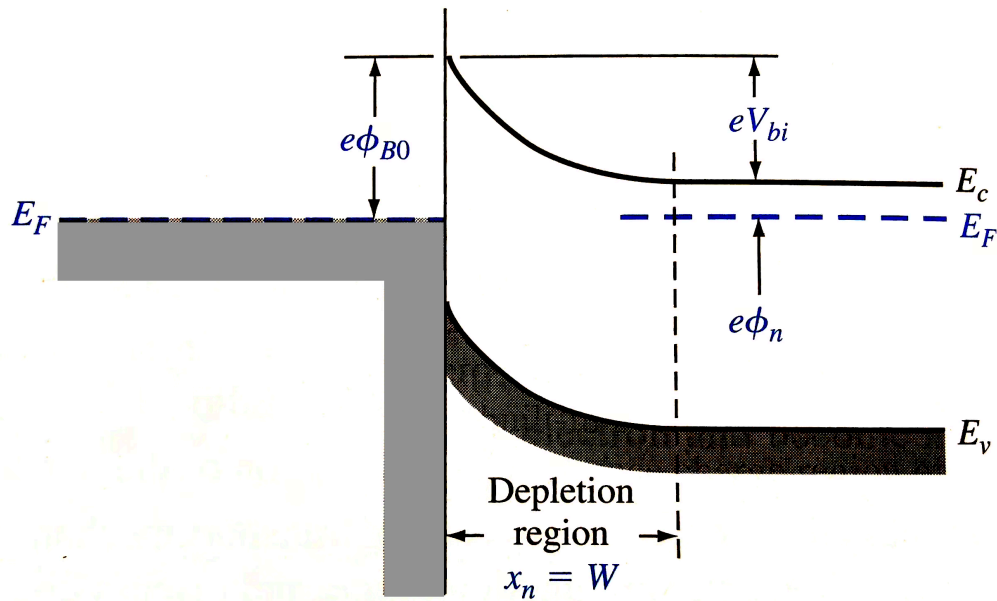


Figure 9: Band structure of metal-semiconductor Schottky contact¹²

For a carrier to travel from the semiconductor into the metal, it must overcome both the Schottky barrier and the built-in voltage, V_{bi} , of the semiconductor. Proper biasing of

the device will lower the built-in voltage but will not affect the Schottky barrier. Regardless, the right bias (either forward or reverse depending on the semiconductor) will still allow majority carrier electrons to reach the metal more easily.

For the 2D PV devices described above, the band structure is shown in Figure 10; Schottky contacts on either side of the semiconductor attract holes and electrons.

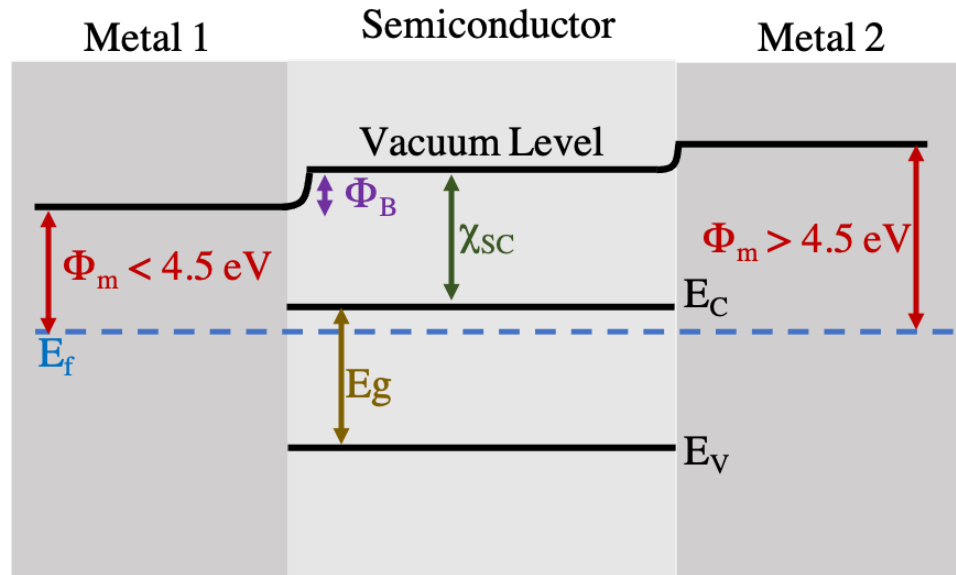


Figure 10: Band structure sketch of a 2D PV device showing the two different Schottky contacts with the semiconductor.

While the ideal barrier height can be easily calculated, there is generally a disparity between the actual and theoretical values. These differences are a result of defects in the crystal and at the semiconductor-metal interface.

2. 2D SEMICONDUCTOR DEVICES

2.1. Device Design

In order to better understand the metal-semiconductor interface in our PV devices, we must fabricate transistors with symmetric metal contacts. This will allow for characterization of device transport, metal conductivity, Schottky barrier extraction, and more.

The transistor consists of a source and drain deposited on top of an oxide substrate (in this case, SiO₂). A 1 μm channel separates the transistors. Long metal fingers connect to large pads for electrical probing, as to not damage the delicate devices. Six devices are fabricated on each sample. MoS₂ film is transferred on top of the transistors while the probing pads remain uncovered.

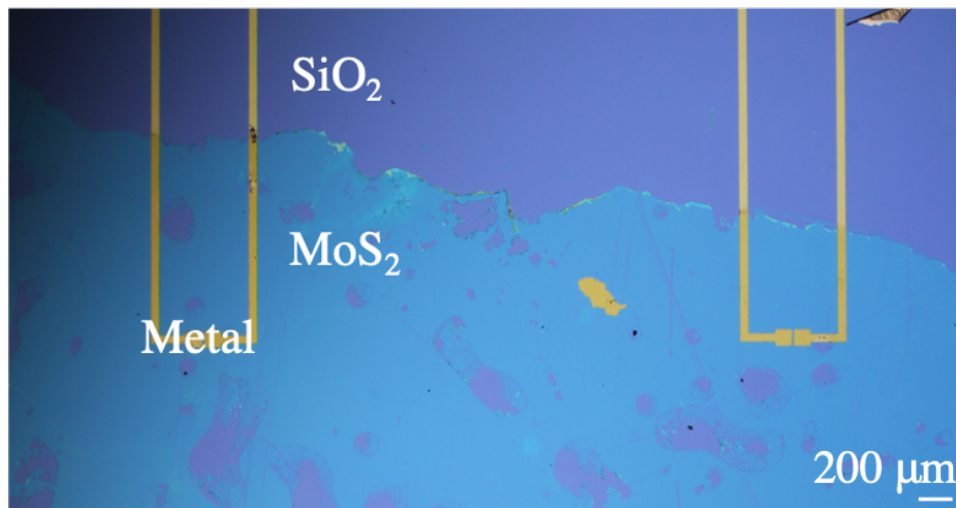


Figure 11: Optical microscope image of transistors with long fingers, with monolayer MoS₂ film transferred on top

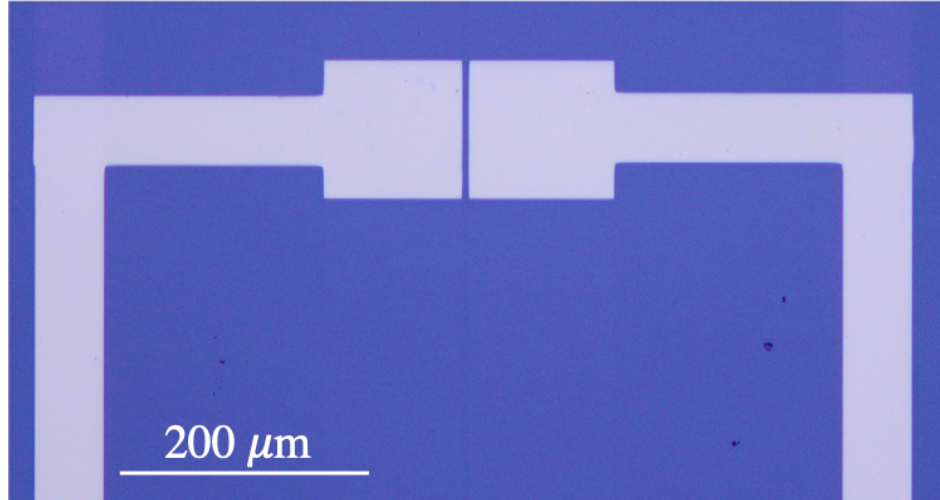


Figure 12: Optical image of 2D MoS₂ transistor, close-up

2.2. Device Fabrication

A SiO₂ (sapphire) substrate is spin coated with PMMA (polymethyl methacrylate) then heated at 180°C for 90 seconds. It is then loaded into an electron beam lithographer (EBL, Raith Nanofabrication) and the devices and contacts are patterned. The developer is applied for 30 seconds, stopped with isopropyl alcohol (IPA), and dried with nitrogen.

The sample is loaded into an electron beam evaporator (E-beam, Angstrom Engineering) and pumped down to 5E-6 – 4E-7 mPa. Through experimentation, we found that Ti adhered to the SiO₂ substrate the best, so a thin layer (5 nm) of Ti is deposited first. Then, 50 nm of the contact metal is deposited. Metals that sublime (Ti, Sc, Pt) use a sweeping beam pattern, while metals with higher thermal conductivity (Au) are deposited using a stationary beam. The sample is removed and goes through liftoff, where it is soaked in acetone and IPA to dissolve the underlying PMMA and leave behind only the contacts and devices. The MoS₂ film is then transferred on top of the devices.

3. CONTACT ENGINEERING

3.1. Metal Selection

For a high-performing PV device, carrier separation is required. In 2D devices, this can be achieved by using asymmetric metal contacts. One metal with a high work function (≥ 5 eV) acts as the hole collector, while the other with a low function (≤ 4.5 eV) acts as the electron collector. The performance of a device is improved with a larger difference between the work functions. For example, a Ti-Pt device will have worse carrier separation and transport than a Sc-Pt, since titanium's work function is closer to that of platinum. Because of this, we investigated integrating new metals into existing PV device designs to compare the electrical performance. Table 2 shows the work functions of commonly used metal contacts.

Metal	Work Function
Platinum	5.4
Gold	5.28
Palladium	5.22
Titanium	4.33
Aluminum	4.08
Scandium	3.5
Yttrium	3.1

Table 2: Metals and their work functions⁴

There are other factors that must be considered when choosing metals to test. Titanium and scandium both oxidize at room temperature, which necessitates extra steps in the

fabrication process to avoid unusable devices. Yttrium and scandium both have to be stored in a sealed glovebox. Gold and platinum are precious metals and therefore cost more. Platinum and scandium both exhibit poor adhesion to SiO₂, so they require a thin layer of titanium to be deposited first.

3.2. Schottky Barrier Extraction

To better understand the metal-semiconductor interface of our devices, the Schottky barrier is extracted. The goal here is to compare the theoretical and extracted value and quantify how defects are impacting the performance of the device. Additionally, the effectiveness of thermal treatments will be quantified by comparing the barrier height before and after processing.

The Schottky barrier extraction relies on the thermionic emission model, which exists in the temperature range where thermal excitation dominates. We consulted numerous Schottky barrier extraction methods ^(4, 5, 6, 7, 8, 9, 10) and adapted our own; the following method is most closely related to the barrier extraction done by the Das group⁴.

First, the device is probed within the Linkam temperature-controlled test stage (LTS420E-P). The chamber is closed and purged using dry nitrogen. The temperature is ramped to 350 K. A gate sweep is conducted over the range -30 – 30 V, while 2 V is applied to the source drain. The I-V curve data is saved, and the temperature is reduced by 25 K. This process is repeated until roughly 150 K; at this point, the I-V plots begin breaking trend and there is significant freezing occurs on the outside of the stage and tubing due to

moisture in the air. After each temperature ramp, the device sits for 5 minutes to allow for thermal adjustment. The temperature-dependent I-V data is plotted in Figure 13.

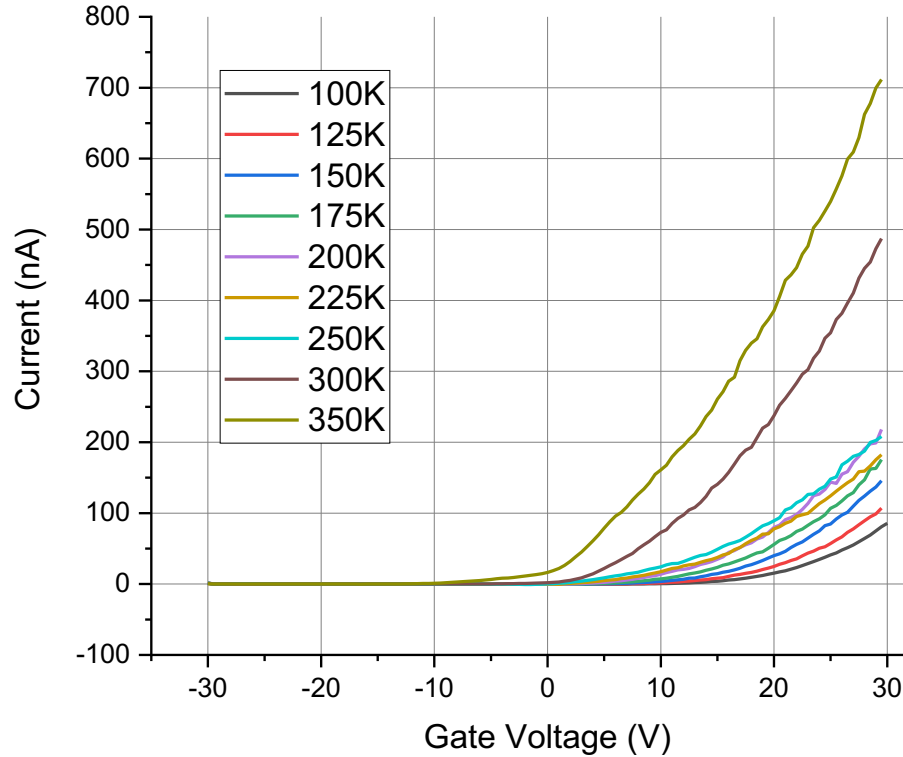


Figure 13: I-V curves resulting from a sweep of the applied gate bias from -30 – 30 V over a temperature range of 350 – 100 K. As expected, current increases with temperature, but will start to decrease around 400 K due to excess thermionic emission.

The source-drain current (I_{SD}) data from the sweep is transposed so that each column represents a certain gate voltage, and each row is a different temperature point. This data is plotted in Arrhenius plot, with $1000/T$ on the x-axis and the natural log of source-drain current on the y-axis. In the high temperature region, the slope of the plot is roughly linear. A linear fit for that portion of the curve is taken for each gate voltage.

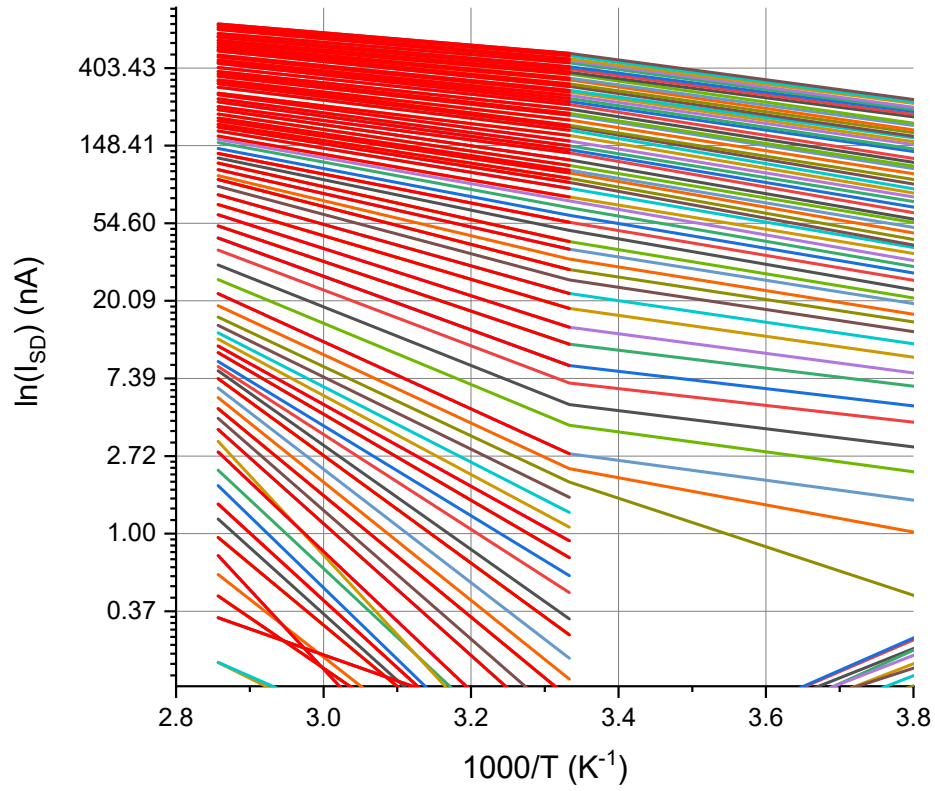


Figure 14: Arrhenius plot of source-drain current and temperature; plot is zoomed in to show the high-temperature region. Red lines indicate the linear fit of the curve over certain temperatures.

This slope is related to the effective Schottky barrier at a given temperature using Equation 3. Here, k_B is Boltzmann's constant, A is Richardson's constant, V_{DS} is the source-drain voltage, and q is the charge of an electron.

$$\phi_B = \frac{k_b T * \ln(I_{SD}/AT^2)}{q * (1 - \exp[qV_{DS}/k_b T])} \quad (\text{Eqn. 3})$$

The effective barrier heights are plotted vs the gate voltage. The point where the curve loses linearity is the flat band voltage (V_{FB}). The y-intercept at this point is the true Schottky barrier height. For the data plotted in the Figure 15, the extracted true Schottky barrier height of Ti-MoS₂ is 0.21 eV.

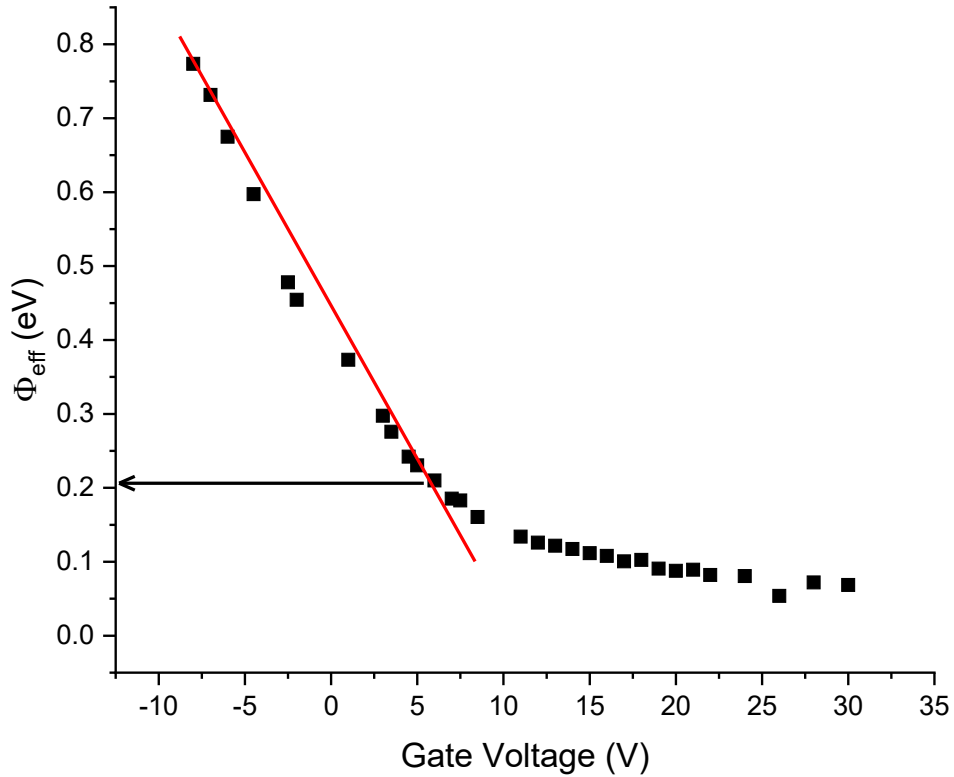


Figure 15: Each effective barrier height is plotted at the respective gate voltage; the plot follows a roughly exponential trend, and the point where initial linearity is broken denotes the transistor turning on, as the Schottky barrier has been overcome.

3.3. Thermal Treatments

Annealing is used to improve interface quality and transport properties. This works by thermally exciting carriers at the interface and causing charge flow in either direction. This allows for mild doping near the interface, mitigating any dangling bonds, trap states, and

other defects introduced in the fabrication process. Additionally, annealing has been found to decrease surface roughness of metal contacts¹⁶, lower specific contact resistance^{17,18}, and improve I-V characteristics¹⁷.

The plan here is to anneal samples at various lengths of time and observe how that impacts the Schottky barrier. Ideally, annealing will cause the difference between the ideal and extracted Schottky barrier to shrink as defects at the interface are reduced. Samples are annealed at 180°C (453.15 K) within the purged Linkam stage to avoid unwanted doping from the ambient environment. Annealing takes place at increments of 5 minutes, not to exceed 1 hour.

4. RESULTS

4.1. Experimental versus Theoretical

To date, the barrier heights of both Ti and Au (no annealing) have been extracted and found to be 0.21 eV and 0.79 eV, respectively.

To gauge how far off the experimental results are, the theoretical values are calculated. Table 3 shows the absolute value of the theoretical Schottky barrier for the four metals being tested. The barrier heights in this table are the offset from the MoS₂'s electron affinity for both the electron and hole carriers, so they must be understood with reference to the band structure in Figure 10. Hole collector (Pt, Au) barrier heights denote how far the metal's Fermi level is below the valence band. Conversely, electron collector (Ti, Sc) barrier heights denote how far the metal's Fermi level is above the conduction band.

Metal	Theoretical Schottky Barrier (eV)
Platinum	1.03
Gold	0.785
Titanium	0.17
Scandium	1.00

Table 3: Theoretical Schottky barriers

4.2. Impact of Annealing on Schottky Barrier

Through limited study so far, it appears that annealing does in fact result in a Schottky barrier closer to the ideal. After annealing a Ti device for 5 minutes, the Schottky barrier dropped by 0.01 eV to 0.20 eV, which is only 0.03 eV off of the target ideal value. This implies that even limited annealing improves the interface and causes the device to trend towards ideal performance.

4.3. Future Work

There is much forward work to be done with this project. The primary focus now is finishing measurements of the barrier heights for additional metals in Table 2 and further characterizing time-dependent annealing and its impact on the barrier heights. If time allows, these measurements should be retaken with a new set of devices to ensure the results are repeatable. Once the improvements from annealing plateau, new optimization methods can be undertaken. By characterizing additional metals like yttrium and palladium on MoS₂ and investigating both their barrier heights and ease of use for PV device contacts,

this work will significantly boost the overall power conversion efficiency of Schottky-type 2D photovoltaics.

CONCLUSION

The Schottky barrier height extraction method has been optimized for easy experimentation and analysis. We have observed that annealing results in more ideal device behavior, which indicates that it will improve Schottky-contact based 2D PV device quality. Based on the work function of the metals and validated by device modeling, scandium and platinum seem to be the most promising contact pairing for good open circuit voltage, fill factor, and solar cell power conversion efficiency. By selecting the right pair of metal contacts and overcoming the defects introduced in the fabrication process, higher quality 2D photovoltaic devices will be able to be fabricated with confidence.

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